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MaryEllen Dobish
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MaryEllen Dobish
(Signature of person mailing paper or fee)

PATENT APPLICATION

Thomas J. Krutsick

CASE 5

TITLE Field Plated Resistor With Enhanced Routing Area Thereover

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

NEW APPLICATION UNDER 37 CFR § 1.53(b)

Enclosed are the following papers relating to the above-named application for patent:

Specification
10 Informal Sheets of drawing(s)
1 Assignment (s) with Cover Sheet
Declaration and Power of Attorney
Information Disclosure Statement

CLAIMS AS FILED				
	NO. FILED	**NO. EXTRA**	**RATE**	**CALCULATIONS**
Total Claims	27 - 20 =	7	x $18 =	$126
Independent Claims	3 - 3 =	0	x $78 =	$0
Multiple Dependent Claims, if applicable			+ $260 =	$0
Basic Fee				$690
			TOTAL FEE	$816

Please file the application and charge **Lucent Technologies Deposit Account No. 12-2325** the amount of $816, to cover the filing fee. Duplicate copies of this letter are enclosed. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 12-2325** as required to correct the error.

The Assistant Commissioner for Patents is hereby authorized to treat any concurrent or future reply, requiring a petition for extension of time under 37 CFR § 1.136 for its timely submission, as incorporating a petition for extension of time for the appropriate length of time if not submitted with the reply.

Please address all correspondence to **Docket Administrator (Room 3C-512), Lucent Technologies Inc., 600 Mountain Avenue, P.O. Box 636, Murray Hill, New Jersey 07974-0636.** However, telephone calls should be made to me at 610-712-3784.

Respectfully,

David L Smith
Reg. No. 30592
Attorney for Applicant(s)

Date: 8/30/00

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Field Plated Resistor with Enhanced Routing Area Thereover

Technical Field

This invention relates generally to semiconductor processing technology and more particularly to a field plated resistor to provide maximum routing area over the field plated resistor.

Background of the Invention

Various methods of fabricating resistors on a semiconductor substrate are known. United States patents 4,140,817, 5,548,268, 5,683,928, 5,976,392, 5,989,970, 6,069,398, and 6,093,596, each of which is hereby incorporated by reference, discloses a method of manufacturing resistors.

In an integrated circuit, a metal, such as a trace, passing over the body of a high sheet resistance diffused resistor, can cause variations in the resistance of the resistor when a voltage is applied to the trace. The voltage on the trace could cause a region of the resistor beneath the trace to invert, deplete, or accumulate, which would result in resistance variations in the resistor. Through repeated occurrences, undesirably, a permanent change to the resistance could occur.

One solution has been to not route metal conductors over resistors to obviate the problem. This technique, however, wastes valuable area and causes integrated circuit die employing this technique to be larger in area than integrated circuit die utilizing the area over resistors for routing metal conductors.

Another solution, illustrated in Figure 18, has been to extend over the resistor body the metal trace that connects to a first one of the resistor contacts. The metal extension, known as a field plate, would extend almost to the metal that connects to the second resistor contact, as layout, design, and fabrication rules allow. In this manner, the voltage applied to the first resistor contact will also be applied to the field plate over the resistor body. The second resistor contact is connected to another potential. There remains variation in the resistance of the resistor due to voltages applied to the first contact and field plate, however, at least the voltage is known. A shortcoming of employing a metal field plate is that the area over the resistor body, excluding the contact areas, is not available for routing other metal conductors in the same layer of metal as contacts to the resistor. Of course, metal conductors could be routed over the resistor body in higher layers of metal, as is known in the art.

Yet another solution, illustrated in Figure 19, has been to provide a polysilicon field plate over the body of the resistor. The metal trace that connects to a first one of the resistor contacts is extended to also contact the polysilicon field plate. Using this technique, a portion of the area over the body of the resistor is available for routing other metal conductors in the same layer of metal as contacts to the resistor. Since the metal that connects to the first one of the resistor contacts makes a second contact with the polysilicon field plate, the area of the contact with the polysilicon field plate, as well as any area near the contact with the polysilicon due to layout, design and fabrication rules, is not available for routing other metal conductors in the same layer of metal as contacts to the resistor.

What is needed is a field plate resistor that permits substantially all of the area over the body of the resistor that layout, design, and fabrication rules permit to be available for routing metal conductors in the same layer of metal as contacts to the resistor.

Brief Description of the Drawing

Figures 1 through 16 are a sequence of sectional views through a semiconductor substrate illustrating steps in the method for fabricating an integrated circuit including a field plated resistor with enhanced routing area thereover, in accordance with the present invention;

Figure 17 is a top view of the field plated resistor with enhanced routing area thereover of Figure 16, illustrating one possible routing of traces over the resistor;

Figure 18 is a sectional view of a prior art resistor having a metal field plate; and

Figure 19 is a sectional view of a prior art resistor having a polysilicon field plate.

Summary of the Invention

In accordance with the invention, an integrated circuit includes a field plated resistor having enhanced area thereover for routing metal conductors, formed in the same layer of metal as forms contacts to the resistor, is fabricated by a sequence of processing steps. A resistor having a resistor body and a contact region at each end thereof is formed in an active region of a semiconductor substrate. A first layer of insulative material is formed over the resistor and a window is created through the first layer of insulative material to the resistor body to form a first contact region. A layer of polysilicon is formed over the first insulative layer to define a field plate, the polysilicon field plate being contiguous with the first contact region of the resistor and extending over the resistor body to substantially to the other contact region, as layout, design, and fabrication rules permit. A second insulative layer is formed over the polysilicon layer. Windows are created in the second insulative layer to provide access to the polysilicon field plate and the second contact region. A metal layer is applied and unwanted metal is etched away to provide conductors over the polysilicon field plate of a field plated resistor having enhanced area

thereover for routing metal conductors formed in the same layer of metal as forms contacts to the resistor.

Detailed Description

Figures 1 through 16 are a sequence of sectional views through a wafer or semiconductor substrate 20 illustrating steps in the method of fabricating a field plated resistor 22 with area thereover for routing metal conductors formed in the same layer of metal as contacts to the resistor are formed. The semiconductor substrate in a preferred embodiment is silicon, but the invention is not limited thereto. Other known semiconductor substrates may be used. While fabrication of a p-type silicon resistor is illustrated, the invention is not limited thereto. Although the method disclosed herein illustrates fabrication of a field plated resistor fabricated in the semiconductor substrate with metal contacts fabricated in the first layer of metal, the invention can be used to fabricate field plated resistors with metal contacts fabricated in higher layers of metal.

As shown in Figure 1, a tub or active area 24 in which field plated resistor 22 will be fabricated is developed in semiconductor substrate 20. An n+ implant step over the active area 24, followed by growth of an epitaxial layer of silicon approximately one micron thick, such as by a chemical vapor deposition process, results in a buried n+ layer 28 beneath the resulting upper surface 30 of substrate 20. The size and shape of active area 24 is dependent on the size of the field plated resistor(s) to be fabricated therein as well as the number of devices including field plated resistors contained therein.

A blanket etch step removes oxide (not shown) from upper surface 30 of substrate 20 to provide access to active area 24. Recesses 26, 32, and 34 are etched into the upper surface 30 of substrate 20 such as by a plasma etch process. An n+ implant into the deep collector is

made to form contact 36 within the active area 24 but outside resistor 22. Contact 36 provides electrical access to the buried n layer 28 from upper surface 30. Field oxide is grown in the trenches for isolation, by any known process such as a recessed polybuffered LOCOS process. Simultaneous with growing the oxide, the n+ implant is diffused.

As illustrated in Figure 2, a mask of photoresist (not shown) is patterned over those portions of surface 30 where an implant is not desired. Portions of the active area 24 are implanted with a p+ dopant, such as but not limited to boron, to form resistor body 38. The amount of p-dopant implanted is determined by the resistance resistor 22 is desired to have, as is known in the art. The photoresist is then removed.

Another photoresist layer (not shown) is patterned over surface 30 where an n+ contact enhancement implant is not desired. The n+ contact enhancement implant, as illustrated in Figure 3, forms contact region 36' within contact 36. Contact region 36' is of lower resistance than contact 36 due to the n+ implant. The photoresist layer is subsequently removed. Hereinafter, the depositing, patterning and removal of photoresist or masks will not always be discussed. One skilled in the art would know of the necessity of such steps.

A polysilicon preparation step deposits a layer of insulative material such as TEOS oxide over surface 30 of the entire substrate 20. Oxide layer 40, as shown in Figure 4, is typically 350 angstroms thick. A layer 42 of amorphous polycrystalline silicon having a thickness of approximately 600 angstroms may be deposited by a chemical vapor deposition process over oxide layer 40. A mask is patterned over layer 42 and an emitter window 44 is etched by a plasma etch process through amorphous polycrystalline silicon layer 42 and oxide layer 40 to the silicon of resistor body 38 in preparation of making contact as first contact 46 with resistor body 38.

Figure 5 is a cross sectional view of substrate 20 following a blanket deposition of a layer 48 of polysilicon, typically 3100 angstroms thick, over the amorphous polycrystalline silicon layer 42 by a chemical vapor deposition process. In addition to forming a layer over the amorphous polycrystalline silicon, the layer 48 of polysilicon fills window 44 making contact with resistor body 38 and defining first resistor contact 46. As part of a doped emitter process, layer 48 of polysilicon is implanted as shown in Figure 6 with a p-type dopant, such as but not limited to boron, to form a p-doped polysilicon. Doping the polysilicon could be achieved by other known methods. The implanting step is not required by the invention, but contributes to field plated resistor 22 being fabricated in an existing process without adding additional processing steps. The p-type dopant forms an enhanced contact region 46'in contact 46. Enhanced contact region 46' is of lower resistance than contact 46.

Subsequent to being implanted, layer 48 of polysilicon is hard masked, then etched by a plasma etch process. When layer 48 of polysilicon is etched, not only are unwanted areas of polysilicon layer 48 removed, but also unwanted areas of the amorphous polycrystalline silicon layer 42 and TEOS layer 40 are etched away. The remaining polysilicon, which forms field plate 50, is shown in Figure 7. The remaining portion of layer 48 of polysilicon extends over substantially all of resistor body 38. The doped polysilicon of field plate 50 provides an electrical path to resistor body 38 through the doped polysilicon in window 44 and enhanced contact region 46'. During a heat treatment step, the amorphous polycrystalline silicon layer 42 is turned into and merged with layer 48 of polysilicon forming polysilicon layer 48'. Polysilicon 48' extends over substantially all of resistor body 38, spaced therefrom by oxide layer 40. Due to layout, design, and fabrication rules, polysilicon layer 48' is etched away from the area (on the right side of Figure 7) where another window will be formed.

Another step not required by the invention but present in the existing process forms spacer 52 around the periphery of the polysilicon structures of emitter contacts (not shown) and field plate 50 formed from polysilicon layer 48 or 48'. A layer of insulative material such as TEOS oxide is deposited over the entire substrate 20. A dry etch process removes the unwanted insulative material, leaving spacer 52, as shown in Figure 8, around the periphery of polysilicon structures. Spacer 52 is typically 1500 angstroms in width at surface 30. In the existing process, spacer 52 is placed around the periphery of polysilicon structures to accommodate metal oxide semiconductor devices or self aligned devices fabricated on the same substrate. Spacers 52 self-aligns the second resistor contact 58 and allows greater utilization of the area over the resistor body 38. While not necessary for the invention, this step contributes to fabricating field plated resistors 22 in an existing process without changing or adding process steps.

A surface implant step, illustrated in Figure 9, implants enhanced contact region 36' of the collector contact 36 with an n-type dopant, such as but not limited to arsenic or phosphorus. The implant lowers the resistance of enhanced contact region 36' and collector contact 36. A mask (not shown) is applied to limit the implant to the n tub collector contact, resulting in a n+ deep collector contact that extends down to the buried layer 28.

Yet another step not required by the invention, but present in the existing process, is a base enhancement implant illustrated in Figure 10. In the base enhancement implant, the polysilicon structures of emitter contacts (not shown) and field plate 50 are again implanted with a p-type dopant, such as but not limited to boron, to reduce the resistance thereof. A photoresist mask illustrated as 54 masks regions where the implant is to be prevented. More importantly, a self-aligned p+ implant is achieve in region 56 in resistor body 38 where a second resistor contact 58 will be formed.

As is known in the art, a trench 60 is formed around active area 24 for isolation of electrical and thermal noise. The steps are not illustrated but the final trench 60 is shown in Figure 11. In forming trench 60, a mask is formed and the trench is etched, such as by a plasma etch process. A p+ implant forms an implant region 62 at the bottom of trench 60. A sidewall oxide is applied to the trench and the trench is filled with polysilicon. Heat treatment causes the implanted dopant to diffuse into resistor body 38 beneath window 44 forming contact 46'.

As illustrated in Figure 11, a planarization step applies one or more layers of insulative material such as oxide, collectively illustrated as dielectric layer 66. In a preferred embodiment, a layer of TEOS, a layer of plasma enhanced TEOS, and a layer of boron-phosphorus TEOS are applied. Layer 66 is reflowed in a heat treatment step to smooth the upper surface thereof.

Dielectric layer 66 is masked and etched, such as but not limited to dry etching process to open windows 68, 70, and 72, as shown in Figure 12. Window 68 opens to polysilicon field plate 50. Window 70 opens to p+ region 56. Window 72 opens to the collector contact 36.

As illustrated in Figure 13, a first barrier layer 74, such as but not limited to platinum silicide, may be formed in each of windows 68, 70, and 72. Platinum is deposited over the substrate and heated to react with silicon where in contact therewith. Unreacted platinum is etched away, as is known in the art. First barrier layer 74 in window 68 is formed in field plate 50. First barrier layer 74 in window 70 is formed in the doped silicon in region 56 forming a second contact 76 to resistor 22. First barrier layer 74 in window 72 is formed in the n+ doped silicon of contact 36.

As illustrated in Figure 14, a second barrier layer 76, such as but not limited to tungsten, is deposited over the first barrier layer 74. The second barrier layer 76, when tungsten may be applied such as but not limited to being by a sputtering process, as is known in the art. Additional or fewer barrier layers may be employed.

In preparation of forming conductors or traces, a layer of metal 80, such as but not limited to aluminum or copper, is deposited as illustrated in Figure 15 over the entire uppermost surface, as is known in the art. In the embodiment illustrated in Figure 15 layer 80 of metal is the first layer of metal, however, the invention is not limited thereto. The invention can be used at any level of metal in a multiple metal level process for fabricating integrated circuits.

Unwanted metal in layer 80 is etched away as is known in the art, resulting in the field plated resistor 22 having traces extending thereover illustrated in Figures 16 and 17. Metal layer 80 provides a lead 82 to emitters (not shown) and field plate 50, a lead 84 to second resistor contact 58, a lead 86 to contact 36, and traces 88 of which traces 90 that are routed over resistor body 38 are a subset. Field plated resistor 22 illustrated in Figure 15 represents a portion of an integrated circuit 98 in which resistor 22 is fabricated. Thus, field plated resistor 22 having an enhanced area over the body 38 of resistor 22 is available for routing other metal conductors over body 38 of resistor 22 in the same layer of metal as forms the contacts to the resistor.

Figure 17 is a top view of field plated resistor 22 of Figure 16 showing one possible routing of conductors 90 over resistor body 38. The width 92 of the resistor body 38 is illustrated as being narrower in width than the width 94 of the first resistor contact 46 and second resistor contact 58 at ends of resistor body 38, although the invention is not limited thereto. Substantially all of the area over the resistor body 38 is available for routing traces or metal conductors, subject only to layout, design, and fabrication rules.

A field plated resistor 22 fabricated in this manner has an enhanced area over the resistor body 38 for routing conductors or traces 90. Layout, design, and fabrication rules may be limiting factors in the utilizing the area over resistor body 38 for routing conductors.

The invention may be fabricated in any known process and is easily fabricated in BICMOS (complementary bipolar) process. Not all steps of the process have been included, or not all details of all steps have been included here, but sufficient disclosure for one skilled it the art has been included. The steps disclosed are those used in a polysilicon emitter process. The polysilicon field plate resistor with enhanced area thereover for routing can be fabricated in this process without any additional processing steps. A polysilicon field plate resistor with enhanced area thereover for routing can be fabricated using less than all of the steps in the polysilicon emitter process.

Although the invention has been described as being fabricated on a silicon substrate, the invention is not limited thereto. Any semiconductor could be used. While a p-type doped region resistor has been described, the invention is not limited thereto; the invention may be used to fabricate field plated resistors of other types of dopings.

Claims

1. An integrated circuit including a field plated resistor, comprising:

a resistor formed in a substrate, the resistor having first and second contact regions:

a fist layer of insulative material over the resistor, the first layer of insulative material having a window therethrough to the first contact region;

a layer of doped polysilicon over the first layer of insulative material to define a field plate over the resistor, the polysilicon filling the window and making contact with the first contact region of the resistor, the field plate extending over the resistor body to proximate the second contact region;

a second layer of insulative material over the resistor, a portion of the second layer of insulative material covering the field plate, the second layer of insulative material having a first window therethrough to the field plate and a second window therethrough to the second contact region;

metal conductors extending over the polysilicon field plate, the conductors formed in the same layer of metal as forms contacts to the first and second contact regions of the resistor.

2. The integrated circuit as recited in claim 1, wherein the first insulative material is an oxide.

3. The integrated circuit as recited in claim 1, wherein the second insulative material is an oxide.

4. The integrated circuit as recited in claim 1, further comprising:

an insulative spacer formed around the field plate.

5. The integrated circuit as recited in claim 1, further comprising:

an enhanced contact region formed at a polysilicon-substrate interface in the window of the first layer of insulative material.

6. The integrated circuit as recited in claim 1, further comprising:

a first barrier layer formed at a metal-polysilicon interface in the first window of the second layer of insulative material.

7. The integrated circuit as recited in claim 6, further comprising:

a second barrier layer formed at a metal-first barrier layer interface in the first window of the second layer of insulative material.

8. The integrated circuit as recited in claim 1, further comprising:

a first barrier layer formed at a metal-substrate interface in the second window of the second layer of insulative material.

9. The integrated circuit as recited in claim 8, further comprising:

a second barrier layer formed at a metal-first barrier layer interface in the second window of the second layer of insulative material.

10. An integrated circuit including a field plated resistor, comprising:

a resistor formed in a substrate, the resistor having first and second contact regions:

a fist layer of insulative material over the resistor, the first layer of insulative material having a window therethrough to the first contact region;

a layer of doped polysilicon over the first layer of insulative material to define a field plate over the resistor, the polysilicon filling the window and making contact with the first contact region of the resistor, the field plate extending over the resistor body to proximate the second contact region;

a second layer of insulative material over the resistor, a portion of the second layer of insulative material covering the field plate, the second layer of insulative material having a first window therethrough to the field plate and a second window therethrough to the second contact region;

metal conductors in a first layer of metal in the integrated circuit extending over the polysilicon field plate, the conductors formed in the same layer of metal as forms contacts to the first and second contact regions of the resistor.

11. The integrated circuit as recited in claim 10, wherein the first insulative material is an oxide.

12. The integrated circuit as recited in claim 10, wherein the second insulative material is an oxide.

13. The integrated circuit as recited in claim 10, further comprising:

an insulative spacer formed around the field plate.

14. The integrated circuit as recited in claim 10, further comprising:

an enhanced contact region formed at a polysilicon-substrate interface in the window of the first layer of insulative material.

15. The integrated circuit as recited in claim 10, further comprising:

a first barrier layer formed at a metal-polysilicon interface in the first window of the second layer of insulative material.

16. The integrated circuit as recited in claim 15, further comprising:

a second barrier layer formed at a metal-first barrier layer interface in the first window of the second layer of insulative material.

17. The integrated circuit as recited in claim 10, further comprising:

a first barrier layer formed at a metal-substrate interface in the second window of the second layer of insulative material.

18. The integrated circuit as recited in claim 17, further comprising:

a second barrier layer formed at a metal-first barrier layer interface in the second window of the second layer of insulative material.

19. A field plated resistor, comprising:

a resistor formed in a substrate, the resistor having first and second contact regions:

a fist layer of insulative material over the resistor, the first layer of insulative material having a window therethrough to the first contact region;

a layer of doped polysilicon over the first layer of insulative material to define a field plate over the resistor, the polysilicon filling the window and making contact with the first contact region of the resistor, the field plate extending over the resistor body to proximate the second contact region;

a second layer of insulative material over the resistor, a portion of the second layer of insulative material covering the field plate, the second layer of insulative material having a first window therethrough to the field plate and a second window therethrough to the second contact region;

metal conductors extending over the polysilicon field plate, the conductors formed in the same layer of metal as forms contacts to the first and second contact regions of the resistor.

20. The field plated resistor as recited in claim 19, wherein the first insulative material is an oxide.

21. The field plated resistor as recited in claim 19, wherein the second insulative material is an oxide.

22. The field plated resistor as recited in claim 19, further comprising:

an insulative spacer formed around the field plate.

23. The field plated resistor as recited in claim 19, further comprising:

an enhanced contact region formed at a polysilicon-substrate interface in the window of the first layer of insulative material.

24. The field plated resistor as recited in claim 19, further comprising:

a first barrier layer formed at a metal-polysilicon interface in the first window of the second layer of insulative material.

25. The field plated resistor as recited in claim 24, further comprising:

a second barrier layer formed at a metal-first barrier layer interface in the first window of the second layer of insulative material.

26. The field plated resistor as recited in claim 19, further comprising:

a first barrier layer formed at a metal-substrate interface in the second window of the second layer of insulative material.

27. The field plated resistor as recited in claim 26, further comprising:

a second barrier layer formed at a metal-first barrier layer interface in the second window of the second layer of insulative material.

Abstract of the Disclosure

An integrated circuit includes a field plated resistor having enhanced area thereover for routing metal conductors, formed in the same layer of metal as forms contacts to the resistor, is fabricated by a sequence of processing steps. A resistor having a resistor body and a contact region at each end thereof is formed in an active region of a semiconductor substrate. A first layer of insulative material is formed over the resistor and a window is created through the first layer of insulative material to the resistor body to form a first contact region. A layer of polysilicon is formed over the first insulative layer to define a field plate, the polysilicon field plate being contiguous with the first contact region of the resistor and extending over the resistor body to substantially to the other contact region, as layout, design, and fabrication rules permit. A second insulative layer is formed over the polysilicon layer. Windows are created in the second insulative layer to provide access to the polysilicon field plate and the second contact region. A metal layer is applied and unwanted metal is etched away to provide conductors over the polysilicon field plate of a field plated resistor having enhanced area thereover for routing metal conductors formed in the same layer of metal as forms contacts to the resistor.

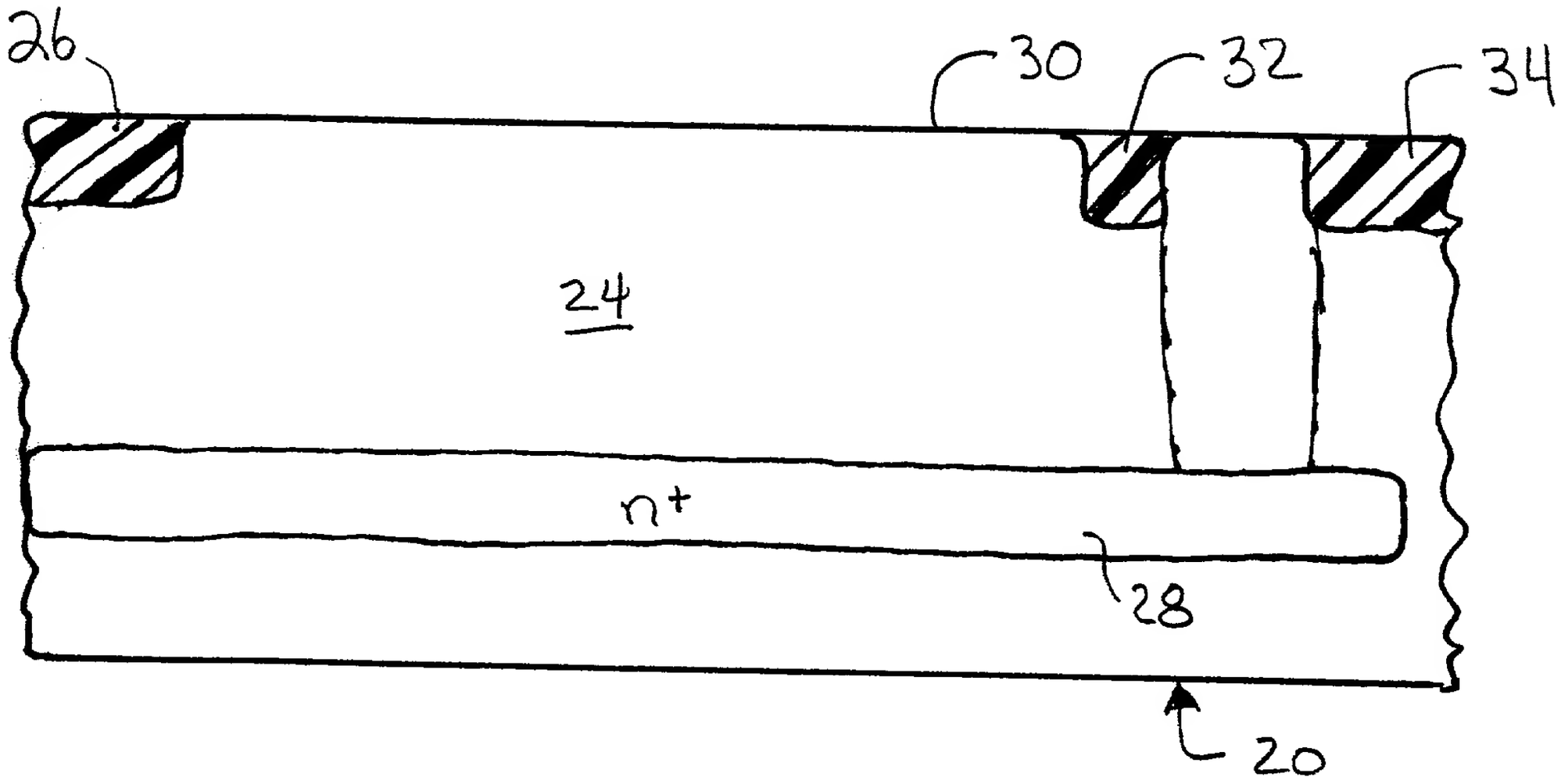

Fig 1

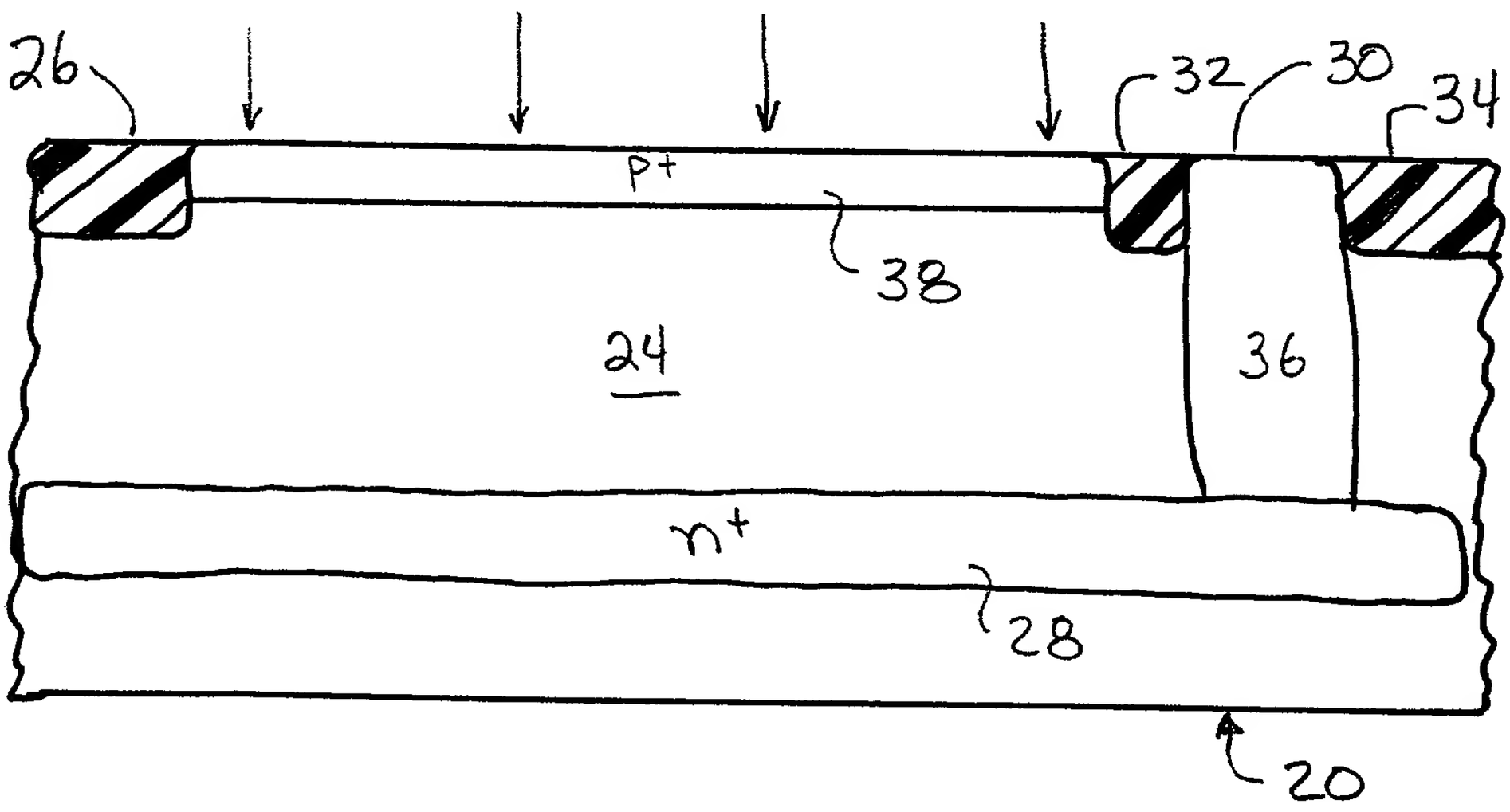

Fig. 2

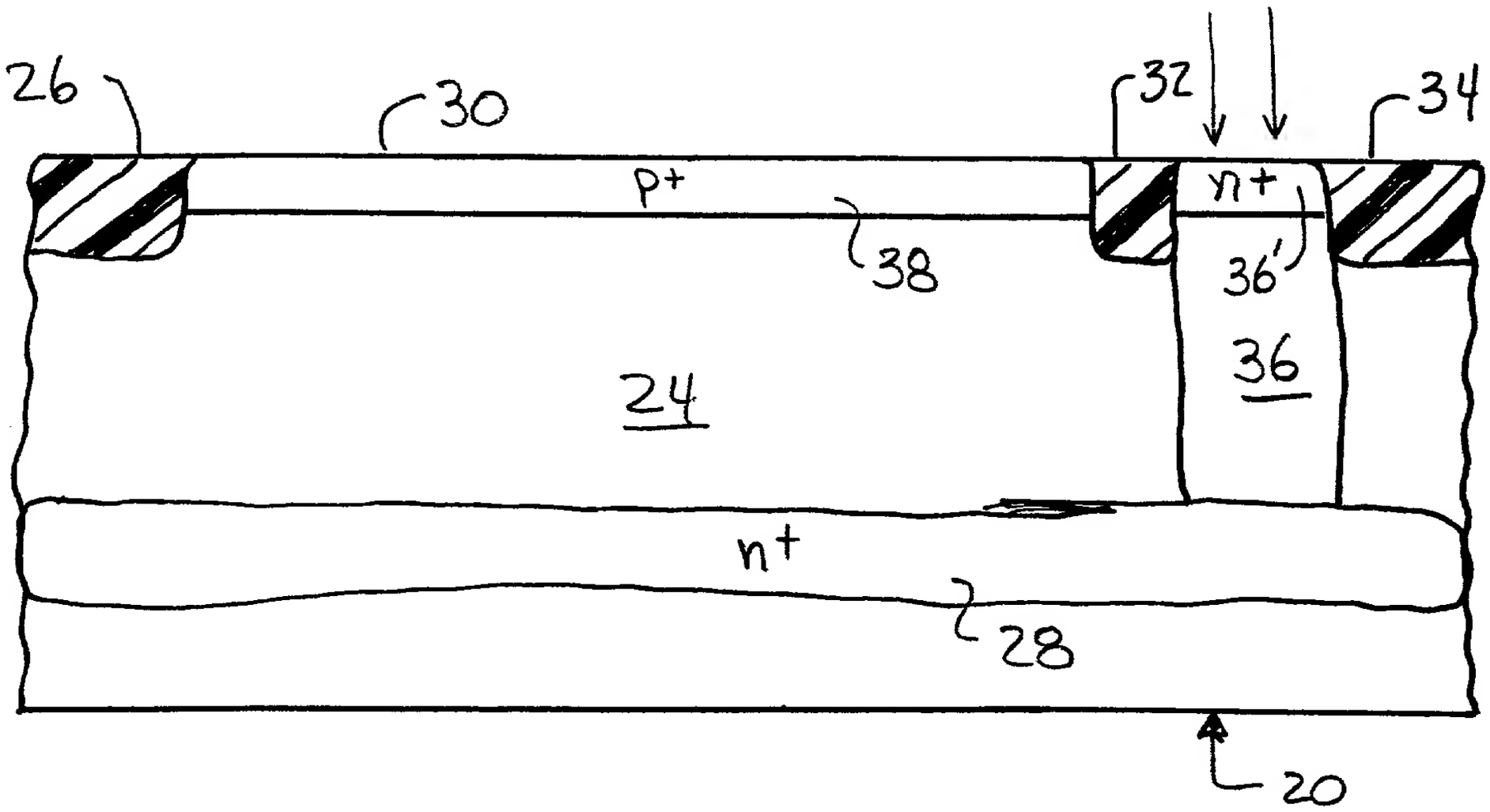
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Fig. 3

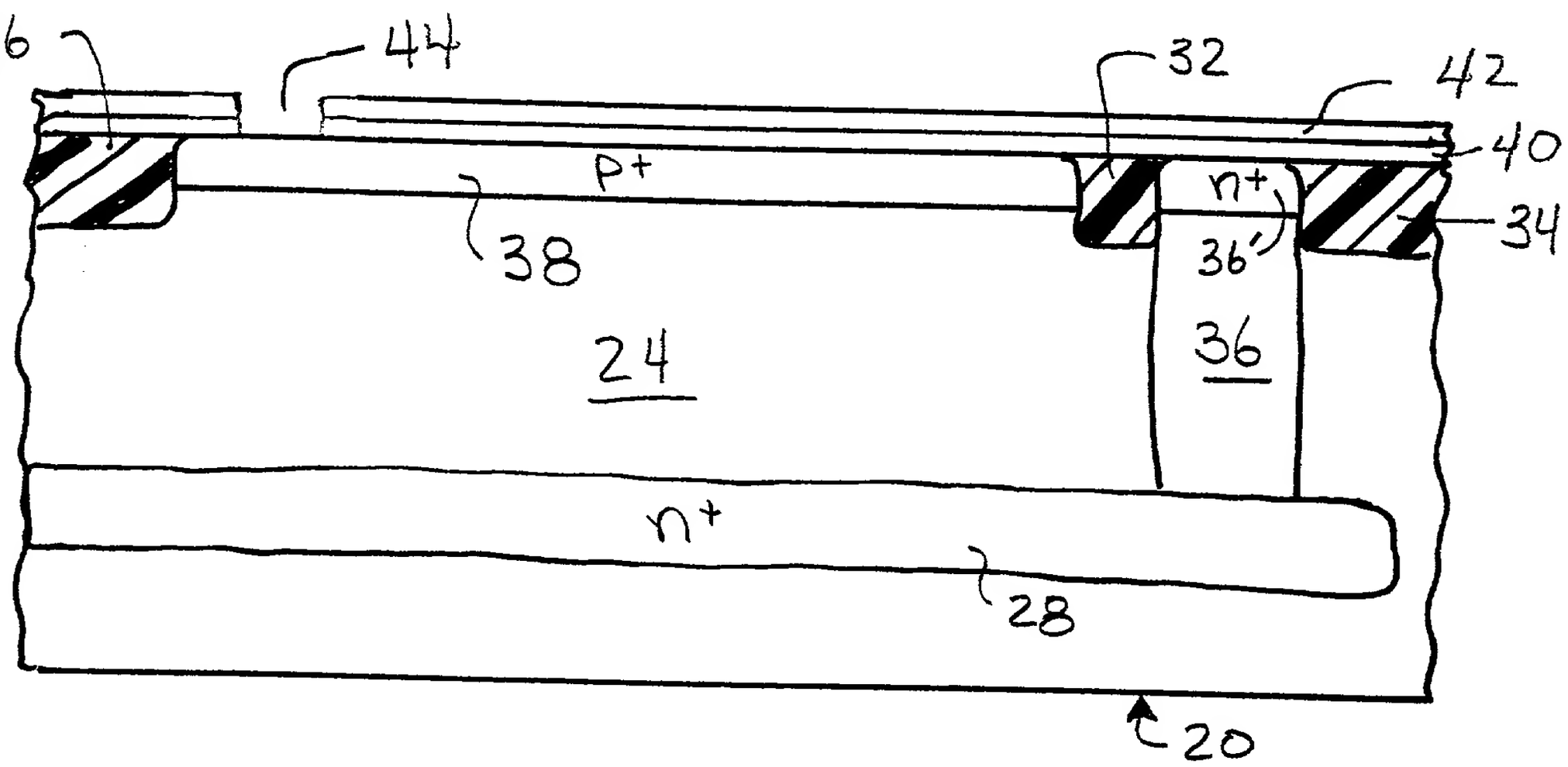
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Fig. 4

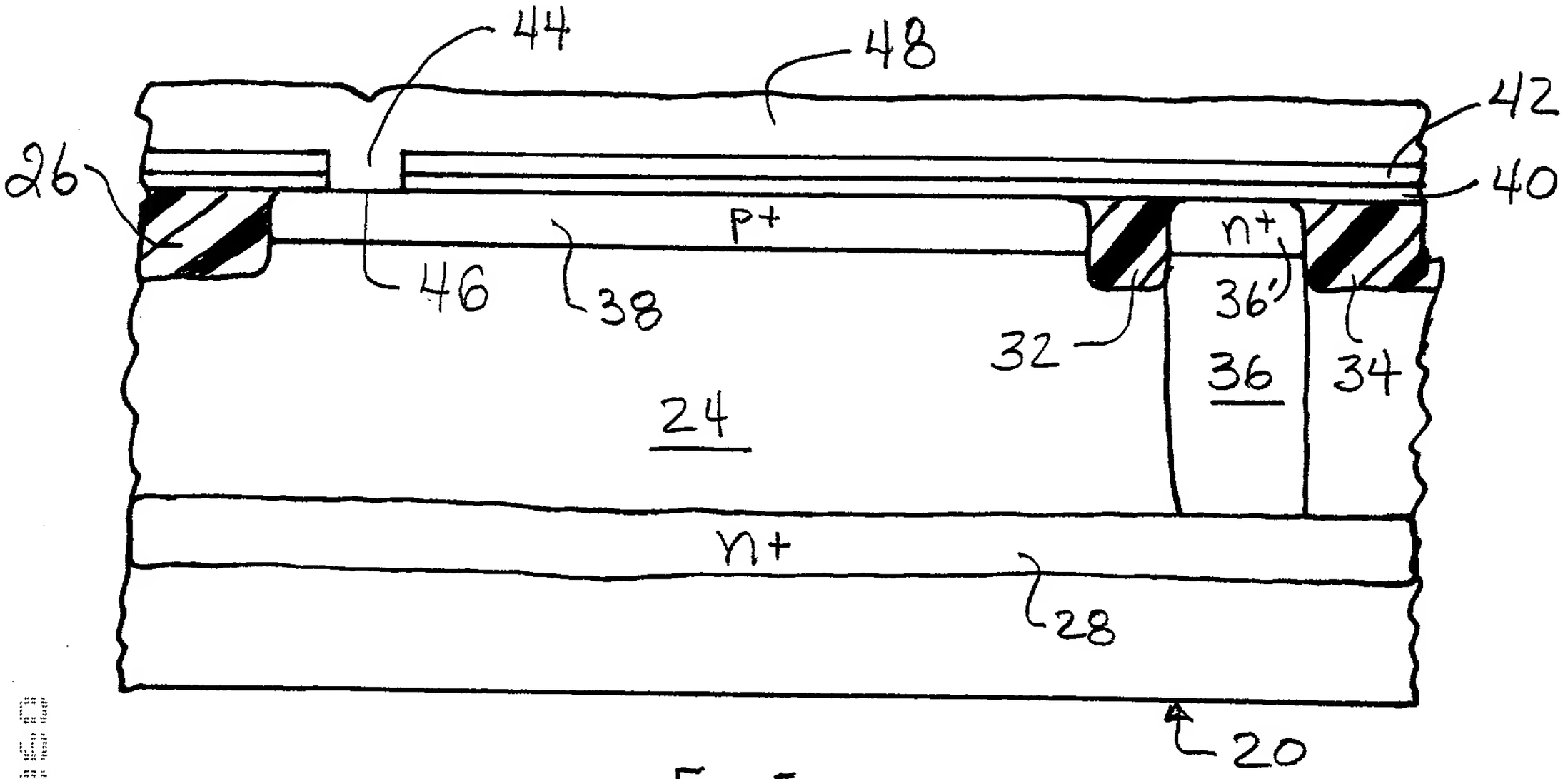
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Fig 5

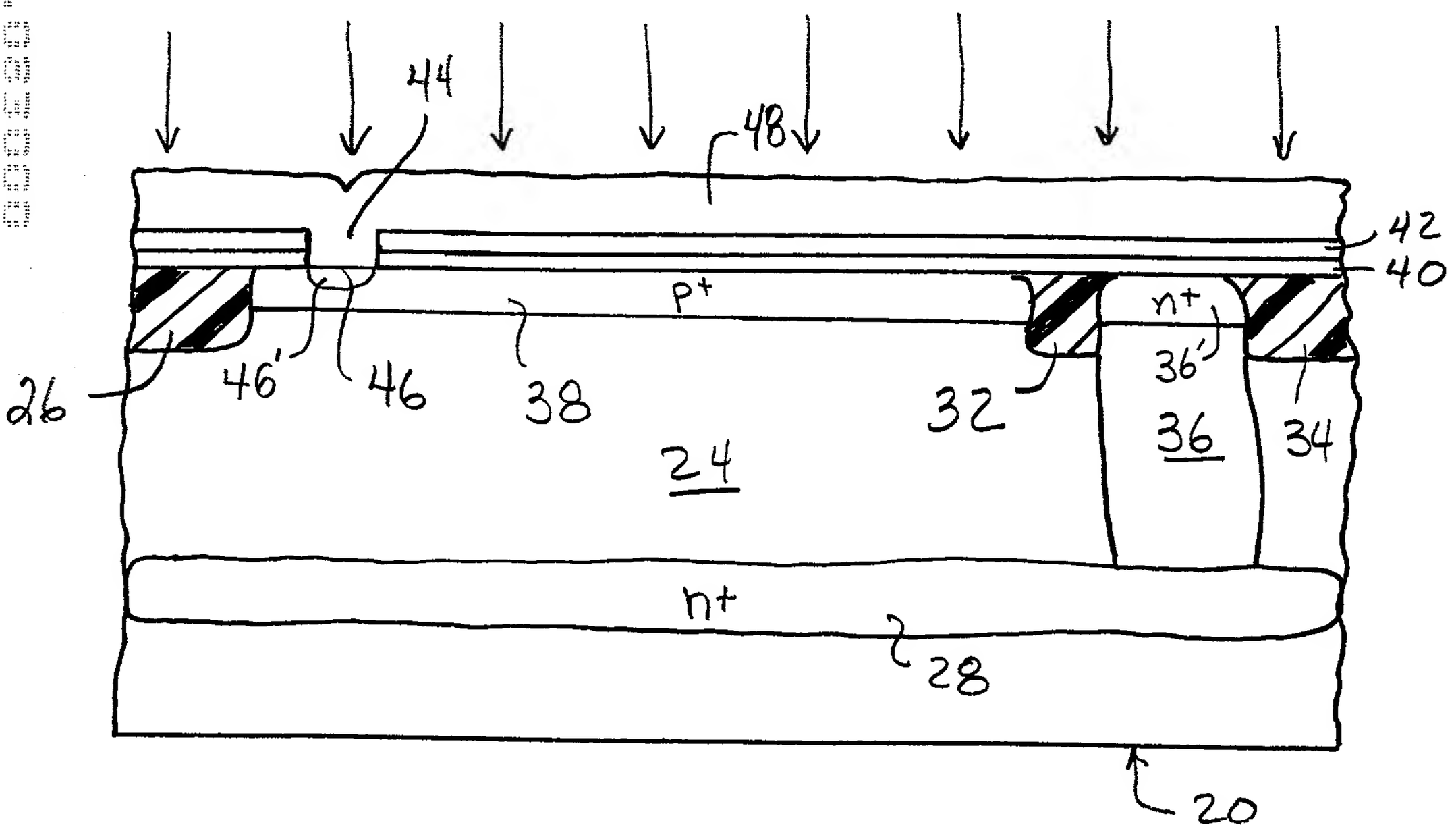
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Fig 6

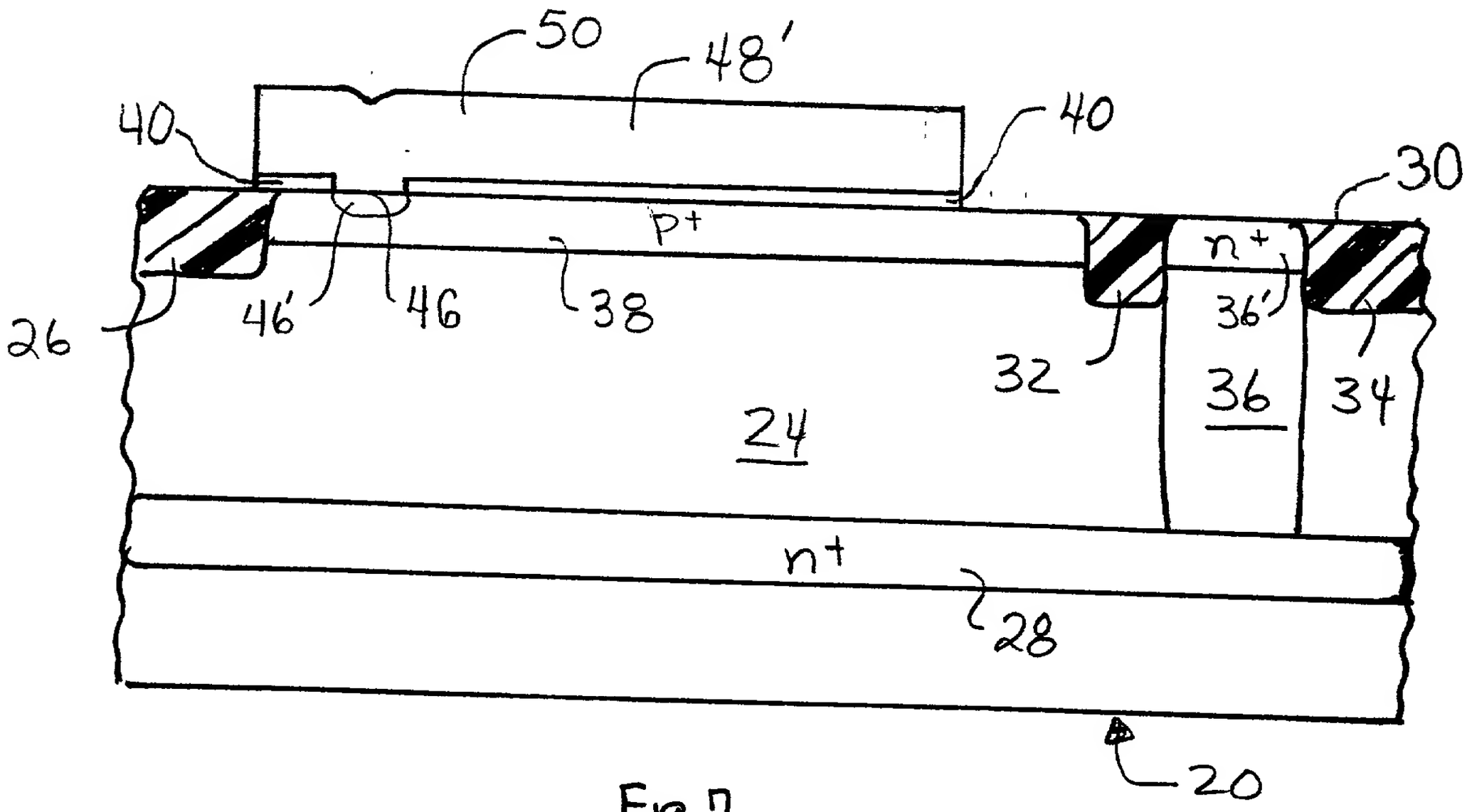
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Fig. 7

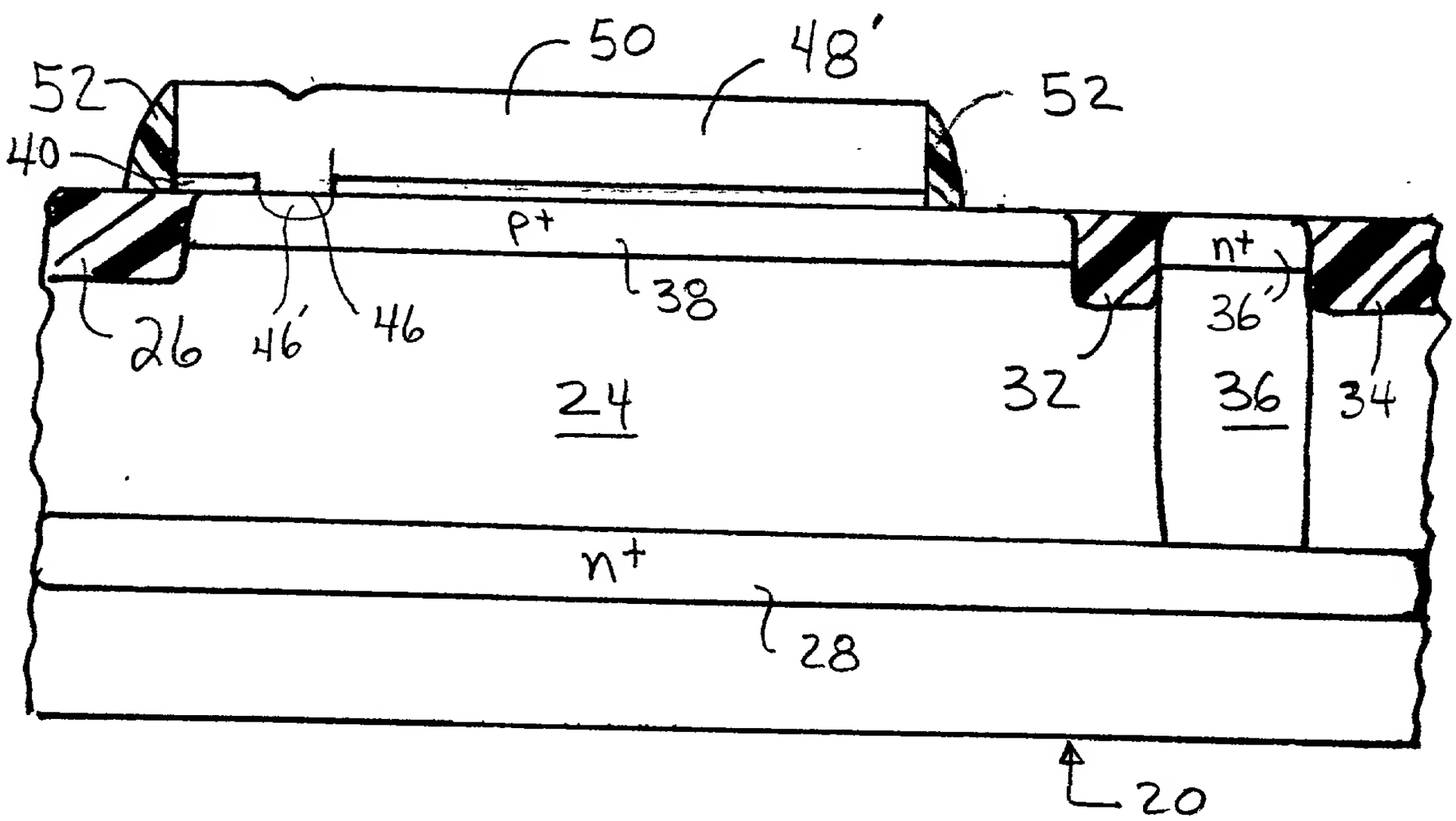
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Fig 8

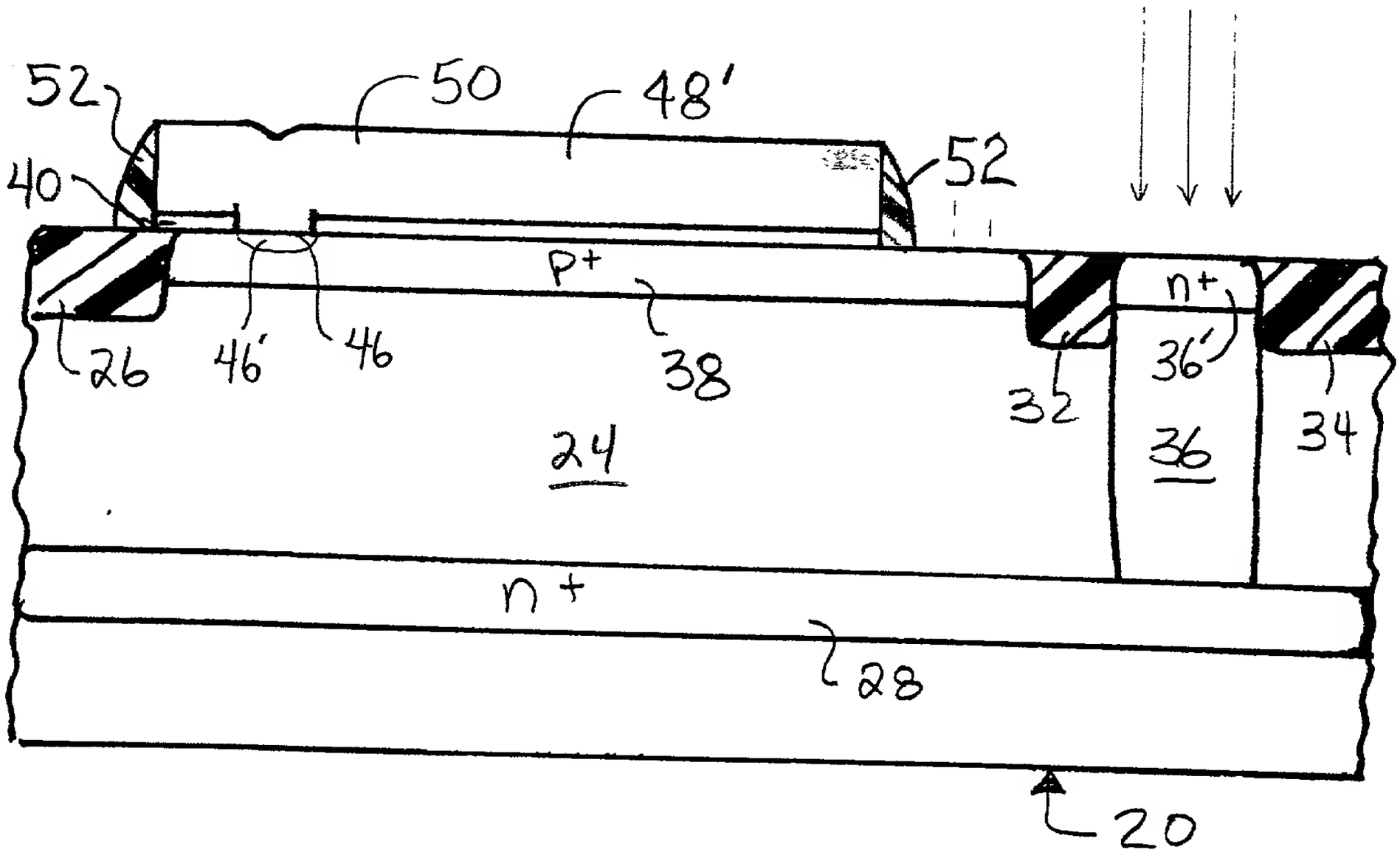
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Fig 9

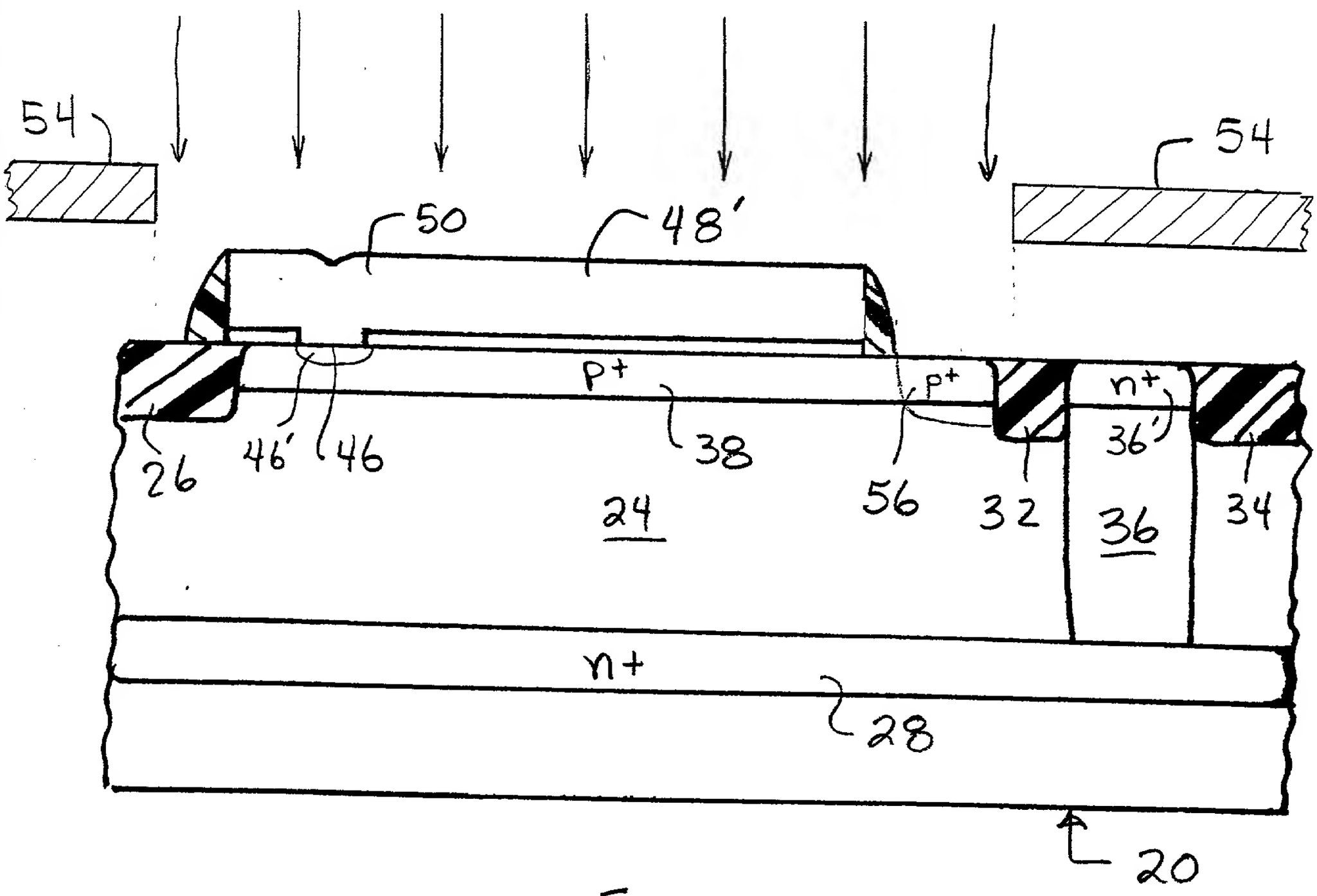
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Fig 10

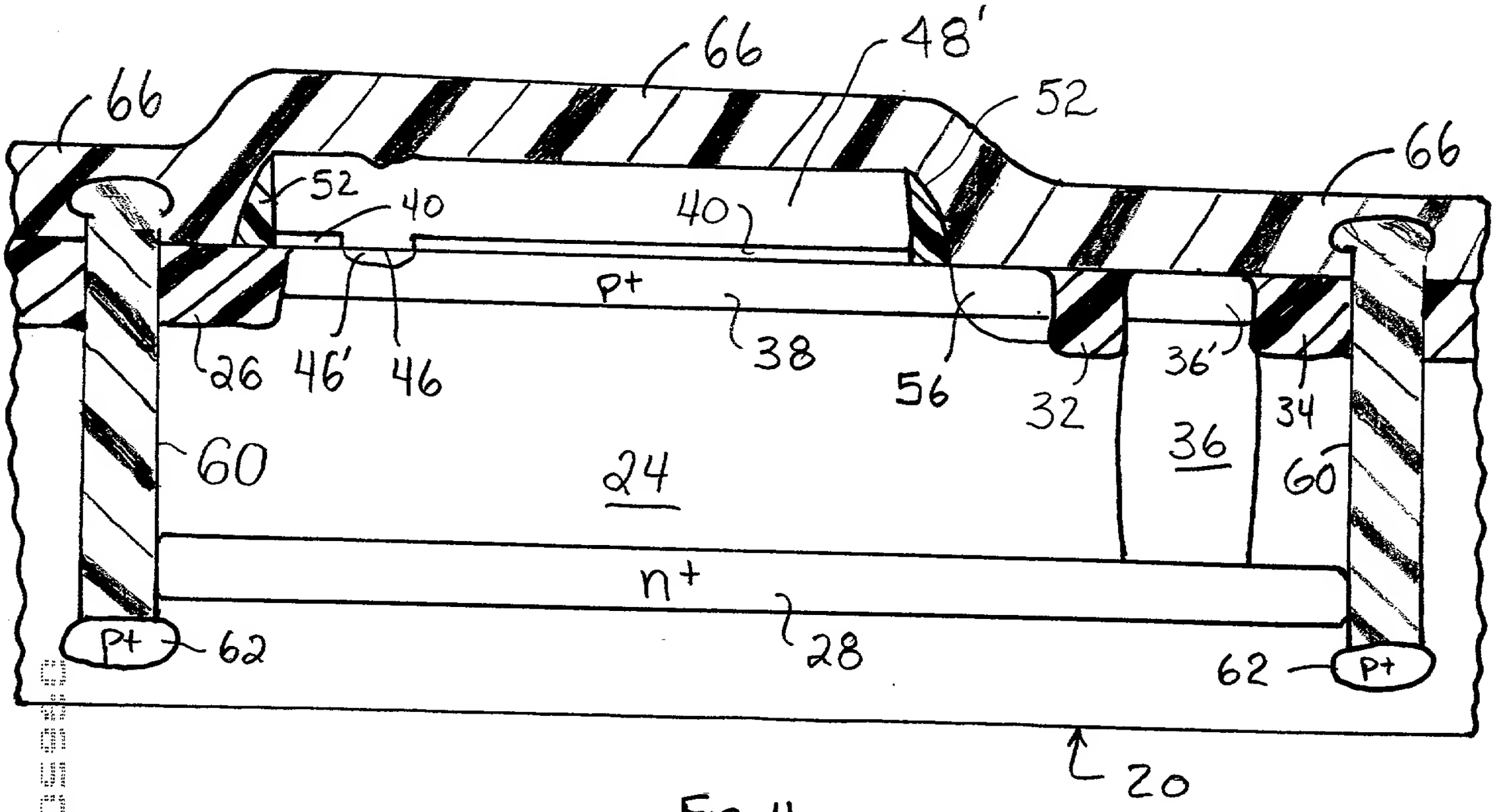

66
66
48'
52
66
52
40
40
P+
26
46'
46
38
56
32
36'
36
34
60
24
60
n+
P+
62
28
62
P+
20

Fig 11

66
68
66
48'
70
66
72
66
52
40
P+
P+
26
46'
46
38
56
32
36'
36
34
24
60
60
n+
P+
62
28
62
P+
20

Fig 12

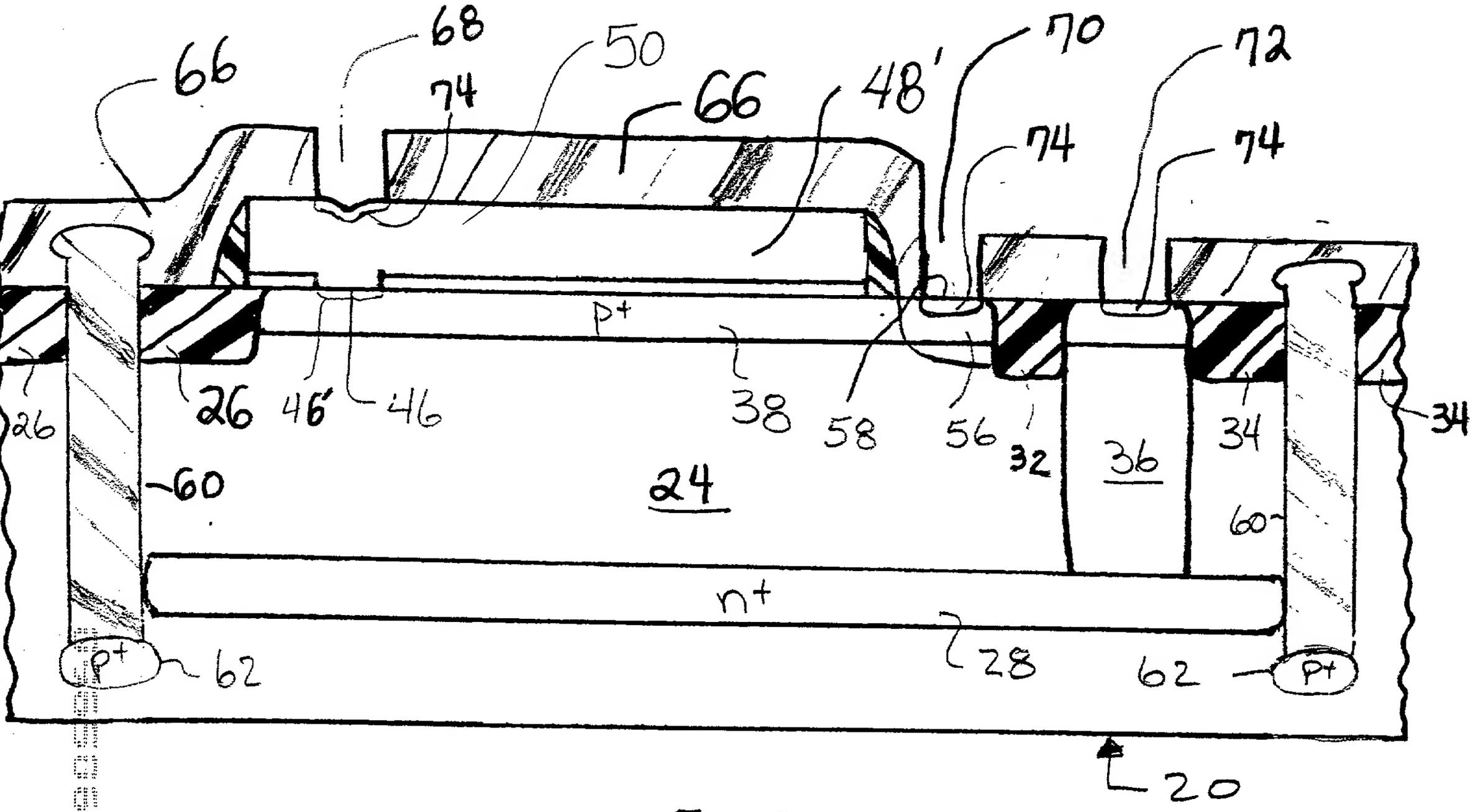

66
68
74
50
66
48'
70
74
72
74
P+
26
46'
46
38
58
56
32
36
34
26
60
24
60
n+
P+
62
28
62
P+
20

Fig 13

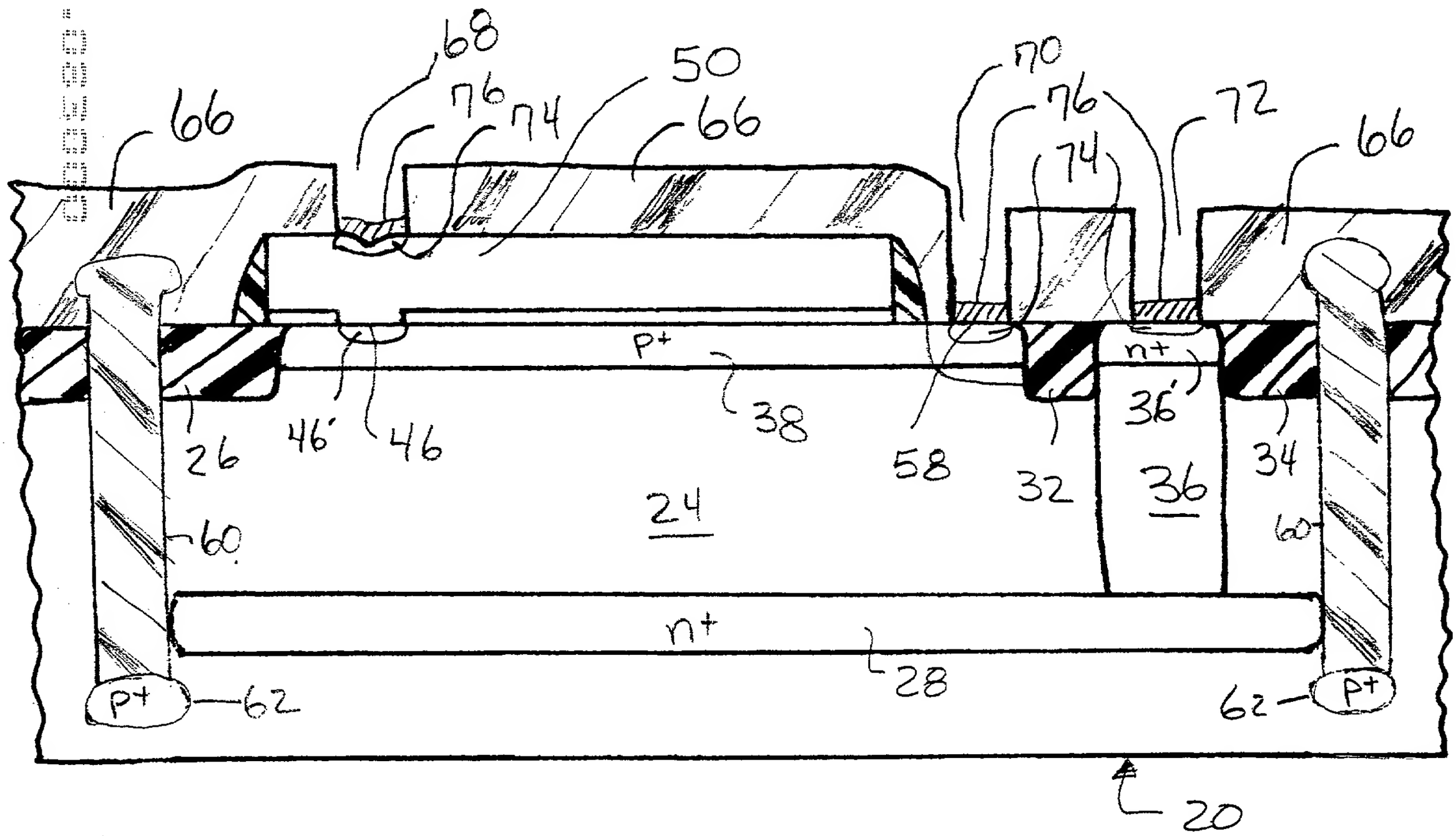

66
68
76
74
50
66
70
76
74
72
66
P+
n+
26
46'
46
38
58
32
36'
36
34
24
60
60
n+
28
P+
62
62
P+
20

Fig 14

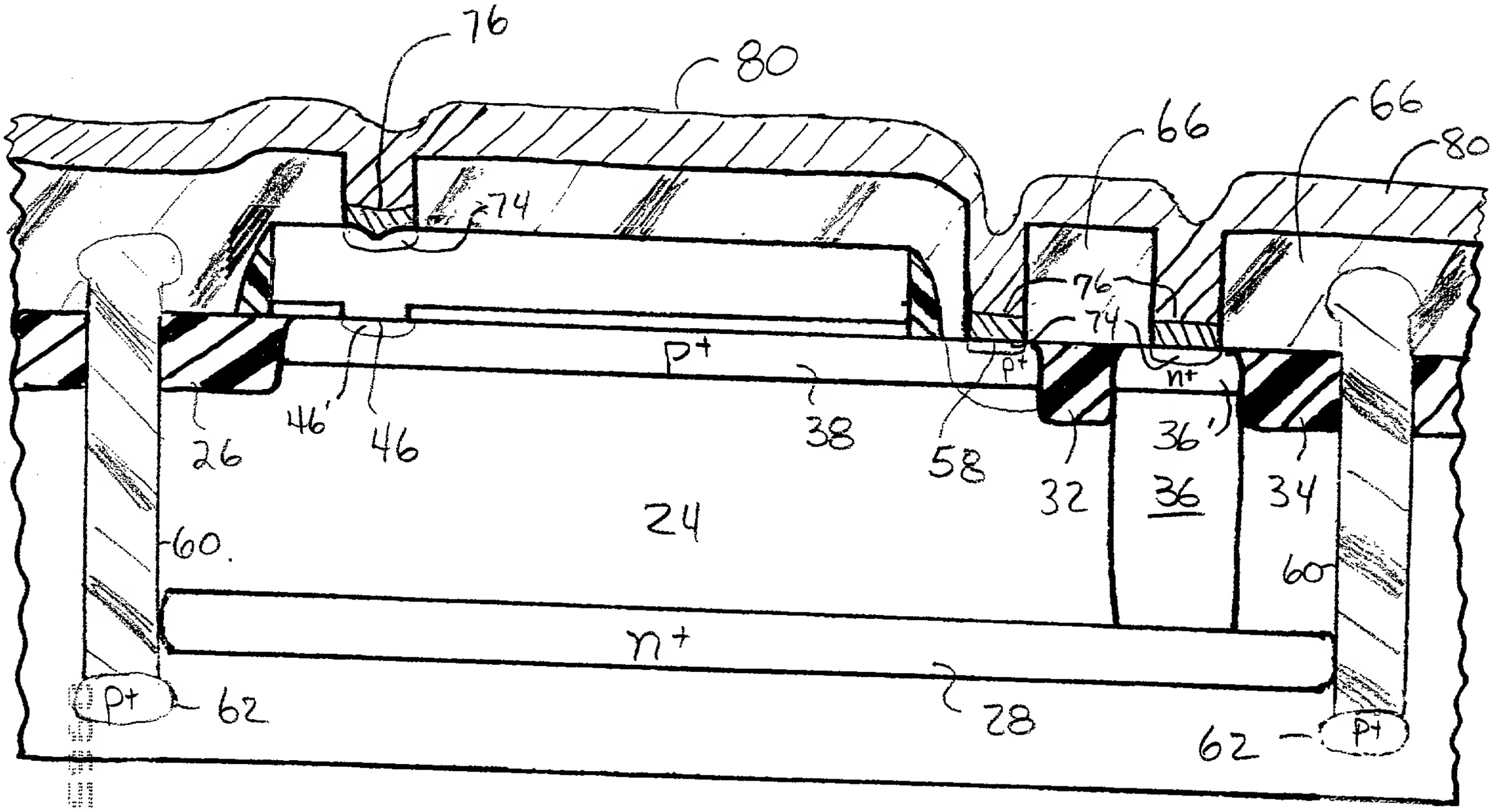

76
80
66
66
80
74
76
74
P+
P+
n+
26
46'
46
38
58
32
36'
36
34
24
60
n+
P+
62
28
62
P+

Fig 15

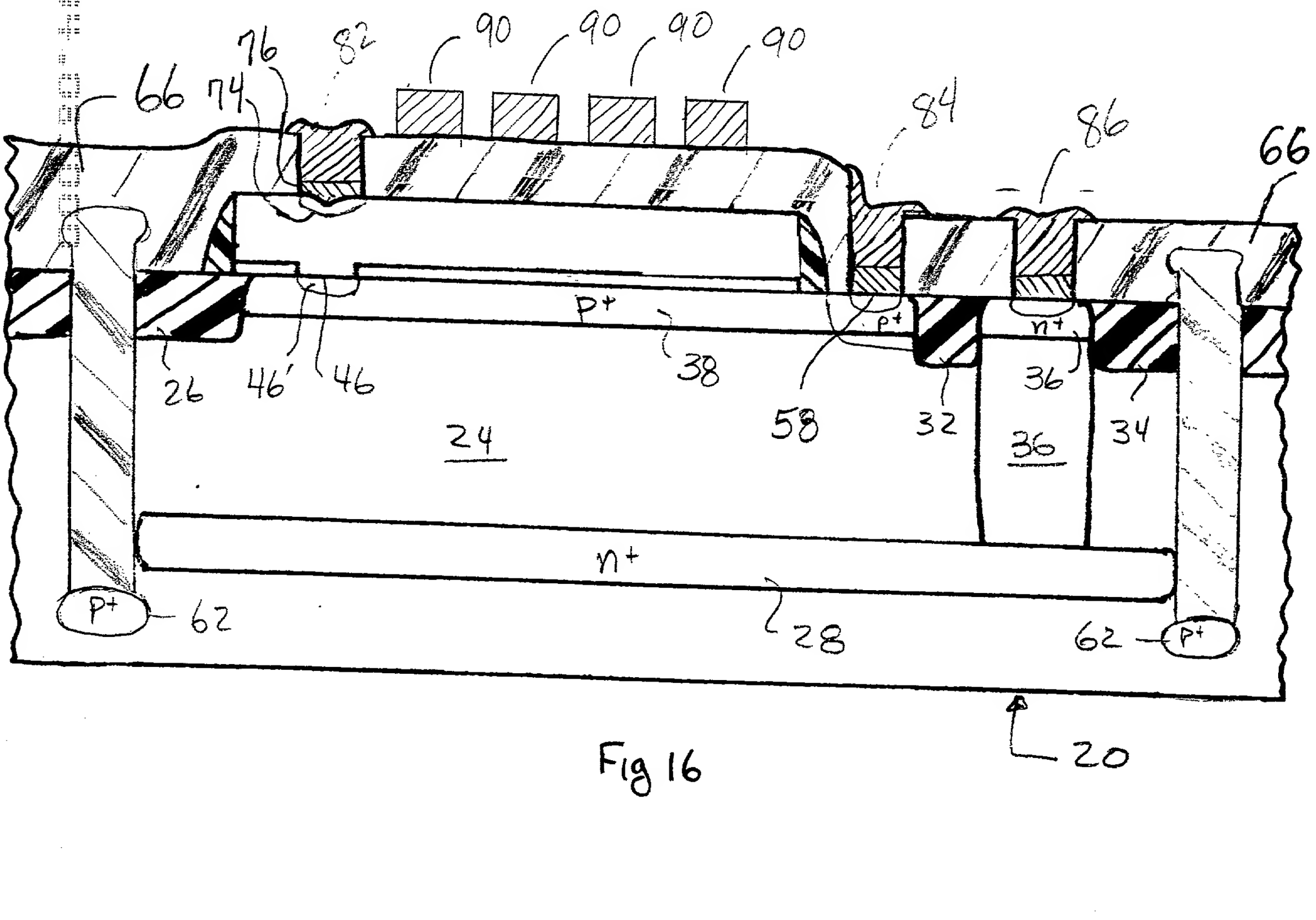

66
74
76
82
90
90
90
90
84
86
66
P+
P+
n+
26
46'
46
38
58
32
36'
36
34
24
n+
P+
62
28
62
P+
20

Fig 16

SH 9/10

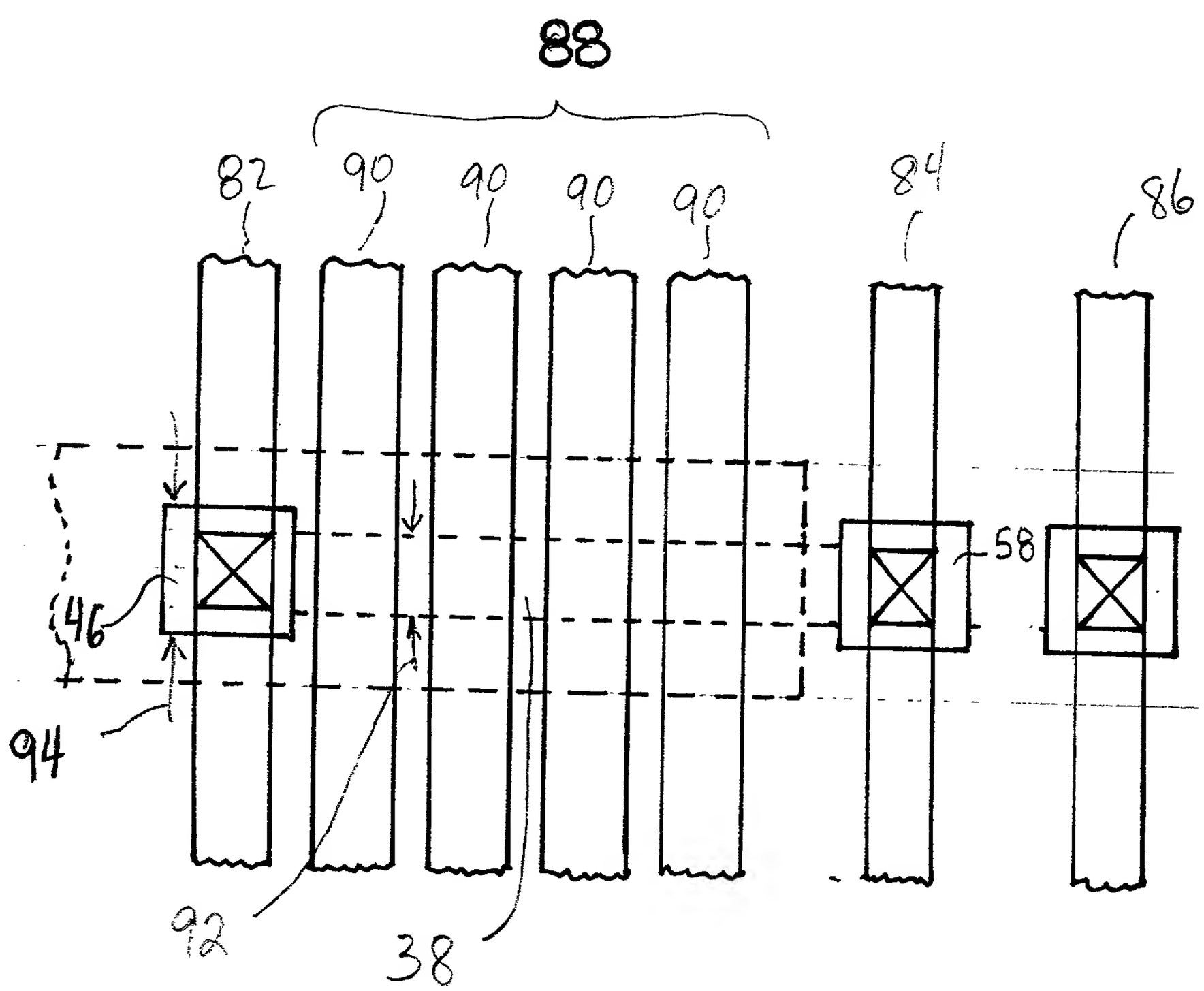
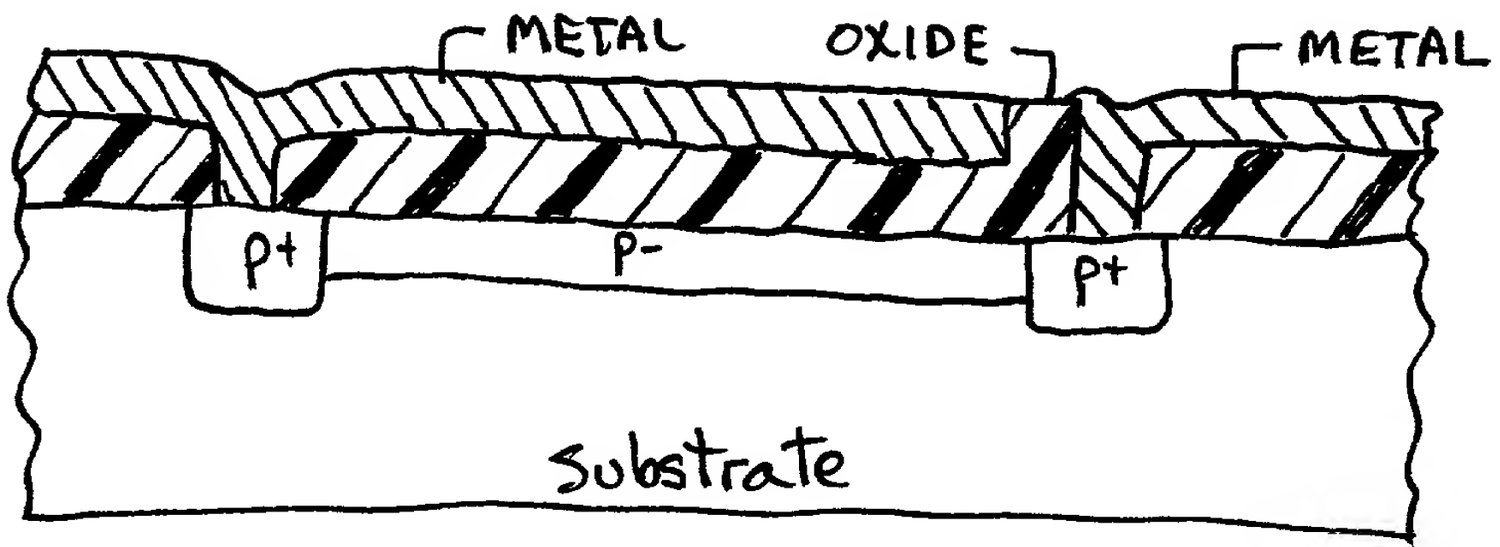
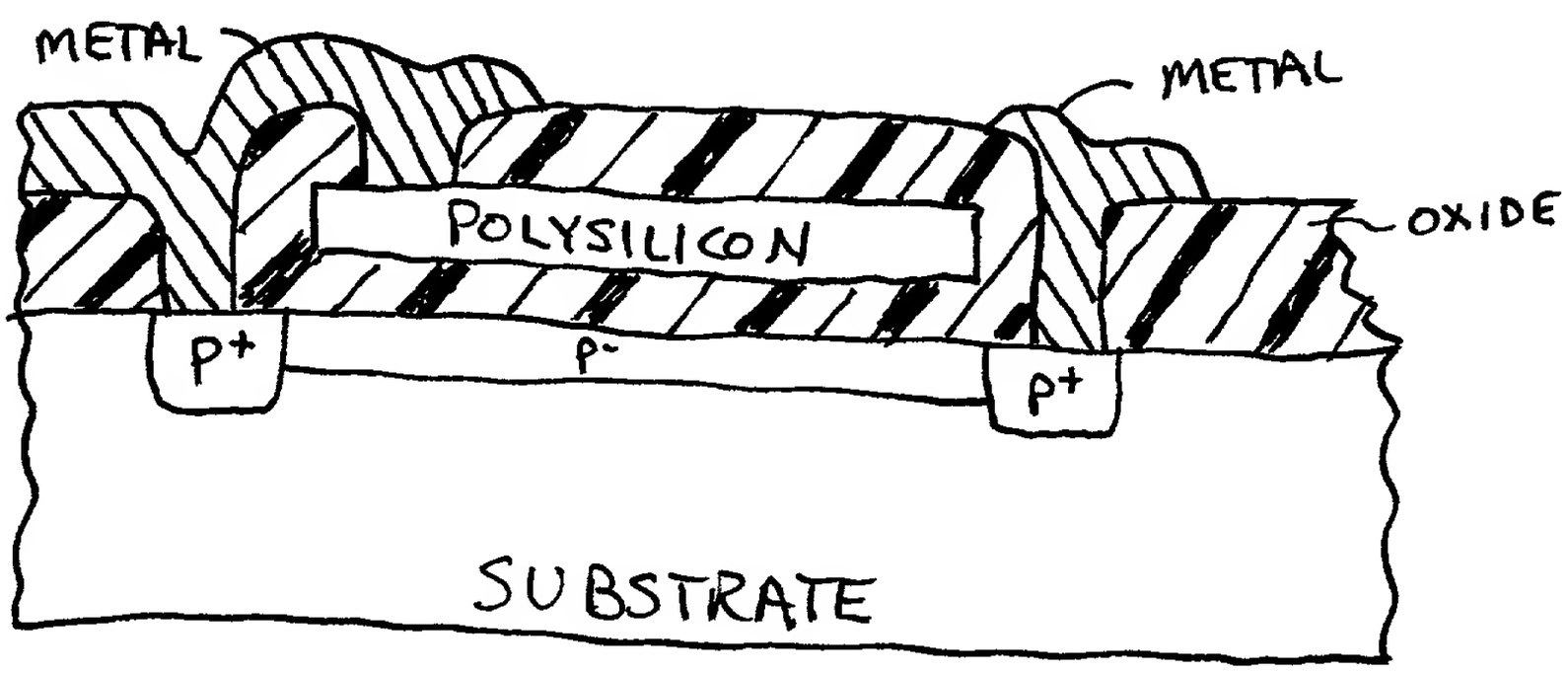


Fig. 17



(PRIOR ART)

Fig. 18



(PRIOR ART)

Fig. 19

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Declaration and Power of Attorney

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **Field Plated Resistor With Enhanced Routing Area Thereover** the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

I hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) with full power of substitution and revocation, to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected therewith:

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